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10/577,133	04/25/2006	Hazuki Okabayashi	P29835	8197
52123 7590 05/25/2010 GREENBLUM & BERNSTEIN, P.L.C. 1950 ROLAND CLARKE PLACE RESTON, VA 20191				
EXAMINER				
SAVLA, ARPAN P				
ART UNIT		PAPER NUMBER		
2185				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com  
pto@gbpatent.com

# Office Action Summary

**Application No.**

10/577,133

**Applicant(s)**

OKABAYASHI ET AL.

**Examiner**

Arpan P. Savla

**Art Unit**

2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 February 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4 and 7-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 7-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/GS/US)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### Response to Amendment

This Office action is in response to Applicant's communication filed February 17, 2010 in response to the Office action dated November 25, 2009. Claims 1-4 and 7-10 are pending in this application.

## REJECTIONS BASED ON PRIOR ART

### Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (U.S. Patent 6,397,298) (hereinafter "Arimilli" in view of Andrew S. Tanenbaum, "Modern Operating Systems, 2nd Edition" (hereinafter "Tanenbaum")).

3. As per claim 1, Arimilli discloses a cache memory which holds, for each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the access order, the cache entry holding unit data for caching, said cache memory comprising:

a modification unit that modifies the order data regardless of an actual access order (col. 4, lines 23-31; Fig. 2, element 24; col. 3, lines 36-37; Fig. 1, element 15);

and a selector that selects based on the modified order data, a cache entry to be replaced (col. 4, lines 12-15; col. 3, lines 36-37; Fig. 1, element 15). *It should be noted that a "cache line" is equivalent to a "cache entry". It should also be noted that the "least-recently-used (LRU)" cache line is replaced.*

Arimilli does not disclose wherein the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset,

wherein said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present,

and wherein said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present.

Tanenbaum discloses the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset (pgs. 216-217, section 4.4.2, R bit); *It should be noted that the "R bit" is equivalent to the "1-bit order flag".*

wherein said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present (pgs. 216-217, section 4.4.2, M bit and Class 1); *It should be noted that the "M bit" is equivalent to the "oldest order-flag".*

and wherein said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present (pgs. 216-217, section 4.4.2, R bit, M bit, and Class 2).

Arimilli and Tanenbaum are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Tanenbaum's Not Recently Used (NRU) replacement algorithm within Arimilli's programmable cache replacement scheme because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of cache entry replacement which is easy to understand and moderately efficient to implement.

4. **As per claim 2**, the combination of Arimilli/Tanenbaum discloses said modifier comprises:

a specifier unit that specifies a cache entry that holds data which is within an address range specified by a processor (Arimilli, col. 4, lines 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15); *It should be noted that the address in cache where the linefill occurs is equivalent to the "address range specified".*

and an oldest-orderer that causes the order data of the specified cache entry to be oldest in the access order, regardless of the actual access order (Arimilli, col. 4, lines

61-65; col. 3, lines 36-37; Fig. 1, element 15). *It should be noted that the linefilled cache line can be given an access status of "LRU" which would mean it becomes "oldest" in order.*

5. **As per claim 7**, the combination of Arimilli/Tanenbaum discloses said modifier modifies the order data so that one cache entry is indicated as an Nth cache entry in the access order (Arimilli, col. 4, lines 61-65; col. 3, lines 36-37; Fig. 1, element 15), wherein N is a number indicating one of: (a) an oldest cache entry in the access order (Arimilli, col. 4, lines 61-65); a number indicating a newest in the access order; an Nth cache entry from the oldest in the access order (Arimilli, col. 4, lines 61-65); and an Nth cache entry from the newest cache entry in the access order (Arimilli, col. 4, lines 61-65). *It should be noted that status "LRU" is equivalent to "oldest in the access order", status "LRU+N" is equivalent to "Nth from the oldest in the access order", and "MRU-N" is equivalent to "Nth from the newest in the access order".*

6. **As per claim 8**, the combination of Arimilli/Tanenbaum discloses said modifier comprises:

an instruction detector that detects that a memory access instruction that includes a modification directive for the access order has been executed (Arimilli, col. 4, lines 23-24 and 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15); *It should be noted that a "linefill operation" is equivalent to a "memory access instruction that includes a modification directive for the access order" because after a linefill the corresponding cache line is always assigned an access status other than MRU.*

and a rewriter the rewrites the order data for a cache entry that is accessed due to the memory access instruction (Arimilli, col. 4, lines 25-31; col. 3, lines 36-37; Fig. 1, element 15).

7. **As per claim 9**, the combination of Arimilli/Tanenbaum discloses said modifier comprises:

a holder that holds an address range specified by a processor (Arimilli, col. 3, lines 44-46; Fig. 2, elements 21); *See the citation note for the first limitation in claims 2 above. It should be noted that the "tag fields" hold the addresses for the cache lines.*

a searcher that searches for a cache entry that holds data corresponding to the address range held in said holder (Arimilli, col. 4, lines 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15); *It should be noted that when a linefill operation occurs it is required the cache lines be searched in order to determine the proper cache line to be updated by the linefill.*

and a rewriter that rewrites the order data so that the access order of the cache entry searched for by said searcher is an Nth cache entry in the access order (Arimilli, col. 4, lines 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15). *See the citation note for claim 7 above.*

8. **As per claim 10**, Arimilli discloses a control method for controlling a cache memory which holds, in each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the access order, the cache entry holding unit data for caching, said method comprising:

modifying the order data regardless of an actual access order (col. 4, lines 23-31; Fig. 2, element 24); *See the citation note for the first limitation in claim 1 above.*

and selecting, based on the modified order data, a cache entry to be replaced (col. 4, lines 12-15).

Arimilli does not disclose wherein the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset,

wherein the cache entry to be replaced is selected when a cache miss occurs and a cache entry having an oldest-order flag attached is present,

and wherein the cache entry to be replaced is selected in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present.

Tanenbaum discloses the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset (pgs. 216-217, section 4.4.2, R bit);

wherein the cache entry to be replaced is selected when a cache miss occurs and a cache entry having an oldest-order flag attached is present (pgs. 216-217, section 4.4.2, M bit and Class 1);

and wherein the cache entry to be replaced is selected in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry



having the oldest-order flag attached is not present (pgs. 216-217, section 4.4.2, R bit, M bit, and Class 2).

Arimilli and Tanenbaum are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Tanenbaum's Not Recently Used (NRU) replacement algorithm within Arimilli's programmable cache replacement scheme because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of cache entry replacement which is easy to understand and moderately efficient to implement.

**9. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Tanenbaum as applied to claim 2 above, and further in view of Pettet (U.S. Patent 6,021,480).**

10. **As per claim 3**, the combination of Arimilli/Tanenbaum discloses said specifier comprises:

a judge that determines whether there is a cache entry that holds data corresponding to each line address from the start line address to the end line address (Arimilli, col. 4, lines 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15).

*See the citation note for the first limitation in claim 1 above.*

The combination of Arimilli/Tanenbaum does not disclose a first converter that converts a starting address of the address range to a start line address that indicates a

starting line within the address range when the starting address indicates a midpoint in line data;

a second converter that converts an ending address of the address range to an end line address that indicates an ending line within the address range when the ending address indicates the midpoint in the line data.

Petty discloses a first converter that converts a starting address of the address range to a start line address that indicates a starting line within the address range when the starting address indicates a midpoint in line data (col. 37, lines 9-18; Fig. 75, element 2616); *It should be noted that the "read align logic" is equivalent to the "first converter"*

a second converter that converts an ending address of the address range to an end line address that indicates an ending line within the address range when the ending address indicates the midpoint in the line data (col. 37, lines 9-18; Fig. 75, element 2616); *It should be noted that the "read align logic" is also equivalent to the "second converter"*.

The combination of Arimilli/Tanenbaum and Petty are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Petty's align logic within Arimilli/Tanenbaum's CPU such that any cache address used by the processor would always be properly aligned to a cache line boundary because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods

with no change in their respective functions, and the combination would have yielded the predictable results of reducing system latency by allowing misaligned memory accesses to be corrected by aligning the data transfer with a cache line boundary.

11. **As per claim 4**, the combination of Arimilli/Tanenbaum/Pettey discloses said oldest-orderer attaches, to the order data, the oldest-order flag which indicates that the access order is oldest (Arimilli, col. 4, lines 61-65; col. 3, lines 36-37; Fig. 1, element 15; Tanenbaum, pgs. 21—217, section 4.4.2, M bit). *See the citation note for the second limitation in claim 2 above.*

#### **Response to Arguments**

12. Applicant's arguments filed February 17, 2010 with respect to **claims 1-4 and 7-10** have been fully considered but they are not persuasive.

13. With respect to Applicant's argument regarding the combination of Arimilli/Tanenbaum's disclosure of "said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present", which appears on page 3 of the communication filed February 17, 2010, the Examiner respectfully disagrees. The Examiner notes that Applicant's argument is based on a weak flag W and the various features of said weak flag W. However, this weak flag W or its various features are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

All that is recited in the rejected claim is an "oldest-order flag". When taking the broadest reasonable interpretation of the term "oldest-order flag" it follows that Tanenbaum's "M bit" reads on an "oldest-order flag" because Tanenbaum's M bit can provide oldest [access] order information. Take for example the situation in which there are two cache entries with one cache entry having M=1 while the other cache entry has M=0. In this situation the M bit acts as an "oldest-order flag" because the cache entry with M=1 is older in terms of when it was accessed compared to the cache entry with M=0. Therefore, Tanenbaum's "M bit" discloses an "oldest-order flag", as simply and broadly claimed by Applicant. Furthermore, Tanenbaum's NRU replacement algorithm of a Class 1 page (i.e. cache entry) (M=1 in a Class 1 page) discloses said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present. Accordingly, the combination of Arimilli/Tanenbaum sufficiently discloses said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present.

14. With respect to Applicant's argument regarding the combination of Arimilli/Tanenbaum's disclosure of "said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present", which appears on page 4 of the communication filed February 17, 2010, the Examiner respectfully disagrees. The Examiner notes that Applicant's argument is based on a

use flag U and the various features of said use flag U. However, this use flag U or its various features are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

All that is recited in the rejected claim is a "1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset". Tanenbaum's "R bit" reads on such a 1-bit order flag because Tanenbaum's R bit indicates that a page (i.e. cache entry) to be replaced has been referenced (i.e. accessed) since each page had been cleared (i.e. reset). Applicant alleges that the use flag U is different from Tanenbaum's R bit because the two bits are reset under different conditions. While it may be true that the two bits are reset under different conditions, the Examiner notes that current claim language does not recite the conditions under which the 1-bit order flag is reset. Again, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore, Tanenbaum's "R bit" discloses a "1-bit order flag", as simply and broadly claimed by Applicant. Furthermore, Tanenbaum's NRU replacement algorithm of a Class 2 page (R=1 and M=0 (i.e. M is not present) in a Class 2 page) discloses said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present. Accordingly, the combination of Arimilli/Tanenbaum sufficiently discloses

said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present.

15. With respect to Applicant's argument in the first and second paragraphs on page 5 of the communication filed February 17, 2010, the Examiner respectfully disagrees. As detailed above in sections 13 and 14 of the current Office action, the combination of Arimilli/Tanenbaum sufficiently discloses the selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present and the selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present. Accordingly, based on the foregoing, the combination of Arimilli/Tanenbaum renders claim 1 unpatentable.

16. With respect to Applicant's argument regarding claim 10, which appears on page 5 of the communication filed February 17, 2010, the Examiner respectfully disagrees. The combination of Arimilli/Tanenbaum renders claim 10 unpatentable for the same reasons as detailed above with respect to claim 1.

17. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that the independent claims are patentable and therefore for the same reasons the dependent claims are patentable. However, as

addressed above, the independent claims are not patentable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

### **Conclusion**

#### **STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

#### **CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, **claims 1-4 and 7-10** have received an action on the merits and are subject of a final action.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan P. Savla/  
Examiner, Art Unit 2185  
May 19, 2010

/Sanjiv Shah/  
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